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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,781	08/16/2002	Jyh-Fong Lin	VIAP0028USA	2576

27765 7590 08/24/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
DRULA, BRIAN F	

ART UNIT	PAPER NUMBER
2652	

DATE MAILED: 08/24/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,781	LIN ET AL.	
	Examiner	Art Unit	
	Brian F. Drula	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 August 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities: The description of figure 3 indicates it is a function block diagram of the waveform adjuster circuit 44 shown in figure 2. The detailed description and the reference numeral in figure 3 indicate it is a function block diagram of the controller 42.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not disclosed in the specification or in figure 3 where the output CTL signal of the controller 42 is generated.

The waveform adjustment circuit 44 is not disclosed in detail. It is not made clear in the specification if the waveform adjustment circuit 44 has the same circuit structure

as the controller 42 in figure 3. It is also not disclosed in the specification or in figure 3 where the output signal of the waveform adjuster circuit 44 is generated.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zhang (US/6285863) discloses an automatic gain control circuit including an attenuator that receives an input signal and outputs a first signal, an amplifier that receives the input signal and outputs a second signal, and a controller that selectively enables one of the attenuator or the amplifier and disables the other.

Zhang fails to disclose the circuit for use in an optical disk drive, the controller connected to the attenuator and the amplifier and enabling and disabling according to the first and second temporary output signals, and a waveform adjuster for receiving the first or second temporary output signal to generate an output signal.

Pietruszynski et al. (US/6141169) discloses a data detection circuit for an optical disk device including an attenuator which receives an input signal from a photodiode, a variable gain amplifier that receives the output of the attenuator, a control block which provides control loops through which low frequency control and input offset compensation may be implemented back to the attenuator and the variable gain amplifier, and a digital equalizer for equalizing and adjusting the output waveform. Pietruszynski et al. further discloses that the signals discussed may be either single ended or differential signals.

Pietruszynski et al. fails to disclose the amplifier receiving the input signal and generating a second temporary output signal, the controller selectively enabling either the attenuator or the amplifier and disabling the other according to the first temporary output signal or the second temporary output signal, and a signal processing method of selecting a first or second temporary signal for adjusting a corresponding waveform to generate an output signal.

Kaku et al. (US/6188654) discloses an apparatus including an automatic gain controller (AGC) that receives an RF input signal from an optical disk device. The AGC controls the amplitude of the RF signal to a predetermined amplitude. Kaku et al. further discloses a drive controller that controls the AGC and an automatic slice level controller as a waveform adjuster that digitizes the output signal.

Kaku et al. fails to disclose an attenuator for receiving an input signal and attenuating the input signal to generate a first temporary output signal, an amplifier for receiving the input signal and amplifying the input signal to generate a second temporary output signal, the controller enabling one and disabling the other according to the first temporary output signal and the second temporary output signal, and a signal processing method including attenuating an input signal to generate a first temporary signal, amplifying the input signal to generate a second temporary signal, and selecting one of the first temporary signal or second temporary signal to adjust a corresponding waveform to generate an output signal.

Hutchins et al. (US/5568465) discloses a signal processor for an optical disk device including an automatic gain control (AGC) circuit with a variable gain amplifier (VGA) that receives an input signal from an optical disk and generates an output signal, a microprocessor as a controller which is connected to the amplifier and controls the amplifier, and an equalizer as a waveform adjuster which adjusts the signal from the AGC circuit.

Hutchins et al. fails to disclose an attenuator for receiving an input signal and attenuating the input signal to generate a first temporary output signal, the controller selectively enabling the attenuator or the amplifier and disabling the other according to the first or second temporary output signal, the waveform adjuster generating an output signal from the first or the second temporary output signal, and a signal processing method for attenuating an input signal for generating a first temporary signal and selecting the first or the second temporary signals for adjusting a corresponding waveform to generate an output signal.

Takeda (US/5574709) discloses an automatic gain control system and information reproduction apparatus for an optical disk device including an automatic gain control (AGC) amplifier that receives an input signal from the optical disk and amplifies the signal to generate an output signal to a differentiator and an operational amplifier as a control means which is connected to the AGC amplifier to enable and adjust the AGC amplifier. The ACG amplifier also outputs the signal to an envelope detector and comparator as a waveform adjuster, the envelope detector outputting an

intermediate value as a slice level and the comparator comparing the AGC amplifier output to the slice level and converting the signal to a binary output.

Takeda fails to disclose an attenuator for receiving an input signal and attenuating the input signal to generate a first temporary output signal, the controller selectively enabling he attenuator or the amplifier and disabling the other according to a first and second temporary output signal, and a signal processing method of attenuating the input signal for generating a first temporary signal and selecting a first or second temporary signal for adjusting a corresponding waveform to generate an output signal.

Muramatsu (US/6747924) discloses an optical disk reproduction apparatus including an RF amplifier that amplifies an RF input signal, a waveform equalization circuit and a slicer as a waveform adjuster that equalizes the output signal of the amplifier and binarized by the slicer to generate an output signal, and a CPU as a controller that controls the waveform equalization characteristics of the waveform equalizer.

Muramatsu fails to disclose an attenuator for receiving an input signal and attenuating the input signal to generate a first temporary output signal, the controller connected to the attenuator and the amplifier for enabling one and disabling the other according to a first or second temporary output signal, and a signal processing method of attenuating the input signal for generating a first temporary signal and selecting a first or second temporary signal for adjusting a corresponding waveform to generate an output signal.

In view of the speculation required to interpret the claims and the rejection under 35 U.S.C. 112, first paragraph, no comment will be made regarding the allowability of claims 1-10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian F. Drula whose telephone number is (703) 605-1157. The examiner can normally be reached on Mon. - Fri., 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T. Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. R. YOUNG
PRIMARY EXAMINER

Brian F. Drula
Patent Examiner
AU2652